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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **SASAKI, Tsutomu et al.**

Group Art Unit: **2188**

Serial No.: **09/745,303**

Examiner: **Kevin L. ELLIS**

Filed: **December 26, 2000**

P.T.O. Confirmation No.: 2061

For: **DATA REPRODUCTION DEVICE**

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SUBMISSION OF APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, Va 22313-1450

June 25, 2004

Sir:

Submitted herewith are an original and two copies of an Appeal Brief in the above-identified U.S. patent application.

Attached please find a check in the amount of $330.00 to cover the cost for the Appeal Brief.

If any additional fees are due in connection with this submission, please charge our Deposit Account No. 01-2340. This paper is filed in triplicate.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP

William L. Brooks
Attorney for Applicants
Registration No. 34,129

WLB/mla
Atty. Docket No. **001715**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF APPEALS

APPEAL BRIEF FOR THE APPELLANTS

Ex parte Tsutomu SASAKI et al.

DATA REPRODUCTION DEVICE

Serial Number: 09/745,303

Filed: December 26, 2000

Group Art Unit: 2188

Examiner: Kevin L. ELLIS

William L. Brooks
Attorney for Appellants
Registration No. 34,129

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
Tel (202) 659-2930
Fax (202) 887-0357

Date: June 25, 2004
Atty. Docket No. 001715

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P.T.O. Confirmation No.: 2061

For: **DATA REPRODUCTION DEVICE**

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, Va 22313-1450

June 25, 2004

Sir:

This is an appeal from the Office Action dated January 7, 2004 (Paper No. 13) in which claims 1-4 were finally rejected.

A Notice of Appeal was timely filed on April 5, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the subject application, which is:

Sanyo Electric Co., Ltd.
5-5 Keihanhondori 2-chome
Moriguchi-shi, Osaka, Japan

Sanyo Technosound Co., Ltd.
1-1, Sanyocho
Daito-shi, Osaka, Japan

II. RELATED APPEALS AND INTERFERENCES

Appellants know of no other appeals or interference proceedings related to the present appeal.

III. STATUS OF CLAIMS

Claims 1-4 have been finally rejected under 35 USC §103(a) as unpatentable over U.S. patent 5,428,579 to Robinson et al. (hereinafter "**Robinson et al.**") in view of U.S. Patent 6,332,196 to Kawasaki et al. (hereinafter "**Kawasaki et al.**").

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. CLAIMS ON APPEAL

A clean copy of claims 1-4 on appeal is attached hereto as Exhibit A.

VI. SUMMARY OF THE INVENTION

The present invention generally relates to data reproduction devices for reproducing data recorded on memory cards, and more particularly to data reproduction devices which are designed to reduce power consumption. (Specification, page 1, lines 6-9)

The data reproduction device of the present invention, according to claim 1 on appeal, includes a control circuit for reading out data recorded on a memory card 8 having a controller 9

mounted thereon, and a data processing circuit 3 for processing the read data and outputting the generated data. (Figure 1; Specification, page 5, line 15 to page 6, line 8)

The controller 9 of the memory card 8 is so constructed that an active mode A is set for reading out the data with a current consumption of a first current value (e.g., 33 mA) in response to memory access of data reading and thereafter automatically follows to a standby mode 5 (e.g., 50 μA) for waiting for next memory access with a non-zero current consumption of a second current value less than the first current value. (Figure 3; Specification, page 6, lines 9-15)

The control circuit comprises a buffer 2 for temporarily storing the data to be read out from the memory card 8, first control means to read out the data from the memory card 8 at a first bit rate (e.g., 8 Mbps) to store the generated data to the buffer 2, and second control means to read out the data stored in the buffer 2 at a second bit rate (e.g., 128 Kbps) less than the first bit rate to supply the read data to the data processing circuit 3, and while the data is intermittently read out from the memory card 8 and stored in the buffer 2 according to the first control means, the data is read out from the buffer 2 according to the second control means. (Figure 2; Specification, page 6, line 20 to page 7, line 15)

VII. THE ISSUE

The sole issue in this appeal is whether the invention, as recited in Appellants' claims 1-4 on appeal, is unpatentable over the combination of **Robinson et al.** and **Kawasaki et al.** under 35 USC §103(a).

VIII. GROUPING OF THE CLAIMS

Rejected claims 1-4 on appeal, rise or fall together because the arguments presented herein are directed only to independent claim 1 on appeal, from which claims 2-4 on appeal, depend.

IX. ARGUMENT WITH RESPECT TO THE ISSUES

A. THE REFERENCES

The Examiner has applied two prior art references, namely, **Robinson et al.** and **Kawasaki et al.**, to reject claims 1-4 on appeal under 35 USC §103(a).

Robinson et al. discloses a flash memory card. One flash memory card has circuitry for providing a ready output signal that indicates a first in time transition from a busy mode to a ready mode by either a first flash memory or a second flash memory of the flash memory card. One flash memory card has a power control register that is used to place certain flash memories in a power down mode. One flash memory card retains information in a power control register from a time prior to the entering of a global power down mode to a time after exiting of the global power down mode. One flash memory card has jumpers for indicating how many flash memories are present on the flash memory card.

Kawasaki et al. discloses a disk control apparatus comprising a disk controller for controlling a circuit which controls read operation for reading data from a disk and a CPU for controlling the circuit and the disk controller. The disk controller comprises a buffer memory for storing data for being transferred between a host and the disk controller and a notification section

for notifying the CPU that a first state in which an all buffer region of the buffer memory is stored with data to be transferred to the host transmits to a second state in which a predetermined space occurs in the buffer region of the buffer memory as a result of transferring data to the host. The CPU comprises a main control section for stopping power supply to the circuit during the first state and for supplying power to the circuit in response to a notification from the notification section.

B. SUMMARY OF EXAMINER'S REJECTIONS

In the Office Action mailed January 7, 2004, the Examiner finally rejected claims 1-4 on appeal under 35 USC §103(a) as unpatentable over **Robinson et al.** in view of **Kawasaki et al**.

In that Office Action, the Examiner urged, regarding claims 1, 2 and 4 on appeal, that **Robinson et al.** discloses the invention substantially as claimed. The Examiner stated that there is a memory card that can operate under two current consumption modes, an active and a standby mode (see col. 2, lines 6-12 and line 50 to col. 3, line 49), and that the memory card operates in the active mode when it is being read or written to and in the standby mode when no operation is occurring to the memory card. The Examiner further stated that the standby mode operates with a non-zero current consumption for a second current value less than the first current value (see col. 9, lines 3-54). The Examiner urged that this results in the same power savings as the present invention. The Examiner admitted, however, that **Robinson et al.** does not disclose the buffer memory that data is read into and that when the amount of data stored in the memory falls below a threshold the memory card is then operated in the active mode, but he applied **Kawasaki et al.** for teaching this feature.

The Examiner urged that **Kawasaki et al.** teaches a buffer that is utilized similarly to the claimed buffer, and asserts that the buffer of **Kawasaki et al.** stores data from a storage device and when the buffer contains sufficient data the storage device is operated in a lower power mode. The Examine further states that when the amount of data falls below a threshold the storage device is operated in an active mode and data is read into the buffer (see Abstract and col. 3, liens 5-45). The Examiner concluded that it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of **Kawasaki et al.** in the system of **Robinson et al.** and provide a buffer between the memory card and the requestor of the data. The Examiner urged that the operation of the memory card would operate in a manner similar to that of the storage device taught by **Kawasaki et al**. The Examiner asserted that when there is sufficient data in the buffer the memory card can be operated in a reduced power state, when the amount falls below a threshold the memory card would be operated in the powered up state (active mode) and data read into the buffer. The Examiner concluded that this arrangement would provide power savings because the amount of time the memory card operated in a powered on state (active mode) would be decreased.

Regarding claim 3 on appeal, the Examiner urged that **Robinson et al.** teaches setting the memory card in the standby mode when there is no memory access within a predetermined period of time (see col. 16, lines 16-24).

C. APPELLANTS' ARGUMENT

Claims 1-4 on appeal are patentable over the combination of Robinson et al. and Kawasaki et al. under 35 USC §103(a).

It is a basic tenet of patent law that to justify the use of a particular combination of prior art references to find a claim unpatentable, there must be a showing that the references themselves embody the specific claimed combination. This teaching was affirmed by the PTO U.S. Patent and Trademark Office Board of Patent Appeals and Interferences in *Ex parte Clapp*, 227 USPQ 972 (P.T.O. Bd. Pat. App. Int. 1985). This principle embodies the same concept propounded by the Court of Appeals for the Federal Circuit in that, not only must there be a teaching in the prior art of the structural elements of appellant's claimed invention, the prior art itself must actually suggest that the structural elements by combined in a similar manner as the claimed invention. See, e.g., *Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985), **vacated on other grounds**, *Dennison Mfg. Co. v. Panduit Corp.*, 475 U.S. 809, 229 USPQ 478 (1986).

Robinson et al. discloses a flash memory card with a power control register that is used to place certain flash memories in a power down mode.

Column 2, lines 6-12 disclose:

> One type of prior flash EPROM used in a prior flash memory card has a standby mode that disables most of the flash EPROM circuitry and reduces device power consumption. The prior flash EPROM also has an active mode. The active mode requires increased power consumption. The active mode is used when the flash EPROM is being written to, read from, or erased.

The Examiner has admitted that **Robinson et al.** does not disclose the buffer memory that data is read into and that when the amount of data stored in the memory falls below a threshold the memory card is then operated in the active mode, as recited in claim 1 of the instant application.

Kawasaki et al. discloses a disk control apparatus comprising a disk controller for controlling a circuit which controls read operation for reading data from a disk and a CPU for controlling the circuit and the disk controller. The disk controller comprises a buffer memory for storing data for being transferred between a host and the disk controller and a notification section for notifying the CPU that a first state in which an all buffer region of the buffer memory is stored with data to be transferred to the host transmits to a second state in which a predetermined space occurs in the buffer region of the buffer memory as a result of transferring data to the host. The CPU comprises a main control section for stopping power supply to the circuit during the first state and for supplying power to the circuit in response to a notification from the notification section.

Kawasaki et al. teaches only one powered state, which occurs only when a predetermined space occurs in the buffer region by transferring data to the host. The other state in which the buffer is completely full of data to be transferred to the host, consumes no power.

This is in contrast to the present invention, in which there are two power on states, where one is a high (active) mode for reading data from the memory card to the buffer at a high bit rate, and the other is a low (standby) mode in which the memory card waits for a next memory access while the buffer outputs data at a low rate.

Neither of the prior art references teaches, mentions or suggests the relationship between the current consumption and the respective data transfer rates of the card and the buffer, as recited in claim 1 on appeal.

In response to this, the Examiner has urged:

> As for applicants remarks regarding the two different bit rates, these rates are only different because the data being read out of the buffer memory is being read out intermittently. As taught by the specification, applicants memory is capable of providing data at 8 Mbps, the data being read out of the buffer is music data that needs to be accessed at 128 Kbps (see pages 6-7 of the specification). Obviously if data is read from a buffer for a storage device at a much slower rate then the data can be read from the storage device then the bit rates will be different. (Office Action of January 7, 2004)

Appellants respectfully disagree. Page 7, lines 1-3 of the specification state that when the memory card 8 is in the active mode, a predetermined amount of data is read from the memory card at a bit rate of 8 Mbps. Page 7, lines 7-9 disclose that, in the stand-by mode, the data read from the memory card 8 is temporarily stored in the buffer 2, and thereafter is read out from the buffer 2 at the bit rate of 128 Kbps.

These passages do not suggest that the data read out of the buffer in the stand-by mode is in intermittent bursts of 8 Mbps to result in an overall rate of 128 Kbps, as asserted by the Examiner. This is because the 8 Mbps rate relates to the output of the memory card 8 while the 128 Kbps rate relates to the output of the buffer 2. Thus, the Examiner's conclusion is based on a false assumption and is not well-taken.

X. CONCLUSION

For the above reasons, The Board of Patent Appeals and Interferences is therefore respectfully requested to reverse the Examiner's rejection of claims 1-4 on appeal under 35 USC §103(a) and instruct the Examiner to pass this application to issue with allowable claims 1-4.

In the event this paper is timely filed, Appellant hereby petitions for an appropriate extension of time. The fee for any such extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP

William L. Brooks
Attorney for Applicants
Registration No. 34,129

WLB/mla
Atty. Docket No. **001715**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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Enclosure: Appendix A containing Claims on Appeal
Petition for Extension of Time

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For: **DATA REPRODUCTION DEVICE**

CLAIMS ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, Va 22313-1450

June 25, 2004

Sir:

The claims on appeal are 1-4, presented below.

Claim 1 (currently amended): A data reproduction device comprising a control circuit for reading out data recorded on a memory card having a controller mounted thereon, and a data processing circuit for giving required processing to the read data and outputting the generated data,

wherein the controller of the memory card is so constructed that an active mode is set for reading out the data with a current consumption of a first current value in response to memory access of data reading and thereafter automatically follows to a standby mode for waiting for next memory access with a non-zero current consumption of a second current value less than the first current value,

wherein the control circuit comprises a buffer for temporarily storing the data to be read out from the memory card, first control means to read out the data from the memory card at a first bit rate to store the generated data to the buffer, and second control means to read out the data stored

in the buffer at a second bit rate less than the first bit rate to supply the read data to the data processing circuit, and while the data is intermittently read out from the memory card and stored in the buffer according to the first control means, the data is read out from the buffer according to the second control means.

Claim 2 (original): A data reproduction device according to claim 1 wherein the first control means starts reading new data when predetermined space capacity is generated in the buffer by the second control means reading out the data from the buffer.

Claim 3 (original): A data reproduction device according to claim 1 wherein the controller of the memory card is so constructed that the standby mode follows when there is no memory access within a predetermined period of time after setting the active mode.

Claim 4 (original): A data reproduction device according to claim 1 wherein the control circuit repeats the intermittent read-out using the buffer until all the data to be reproduced is read out from the memory card.